CLAIMS

WHAT IS CLAIMED IS:

1. An electrical structure comprising:
   a silicon-containing material having a surface; and
   an organic layer chemically bonded to the surface of the silicon-containing material,
   wherein an electrical property of the electrical structure is significantly changed compared to a same structure without the organic layer.

2. The electrical structure of claim 1, wherein the organic layer affects the electrical property within the silicon-containing material.

3. The electrical structure of claim 2, wherein the electrical property is selected from a group consisting of a surface recombination velocity, carrier lifetime, electronic efficiency, voltage, device capacitance, contact resistance, and resistance of a doped region.

4. The electrical structure of claim 1, wherein the organic layer comprises a hydrocarbon.

5. The electrical structure of claim 1, wherein the organic layer comprises a polymer.

6. The electrical structure of claim 1, wherein:
   the silicon-containing material is at least part of a photovoltaic cell; and
   the silicon-containing material comprises a region at the surface, wherein the region has a dopant concentration of at least approximately 1E19 atoms per cubic centimeter.

7. The electrical structure of claim 1, wherein:
   the silicon-containing material is at least part of a channel region of a field-effect transistor; and
   the organic layer is at least part of a gate dielectric for the field-effect transistor.

8. The electrical structure of claim 1, further comprising a high-k material wherein:
   the silicon-containing material is at least part of a channel region of a field-effect transistor;
   the organic layer lies between the silicon-containing material and the high-k material; and
   the high-k material is at least part of a gate dielectric for the field-effect transistor.

9. The electrical structure of claim 1, wherein the silicon-containing material is substantially monocrystalline.

10. The electrical structure of claim 1, wherein the silicon-containing material is polycrystalline.

11. The electrical structure of claim 1, wherein the silicon-containing material is substantially amorphous.

12. The electrical structure of claim 1, wherein a portion of the silicon-containing material immediately adjacent to the organic layer has a porosity no greater than approximately 30 percent.

13. A process for forming an electrical device comprising:
    providing a silicon-containing material having a surface; and
    forming an organic layer chemically bonded to the surface of the silicon-containing material, wherein an electrical property of the electrical device is significantly different compared to a same device if the organic layer is not formed.

14. The process of claim 13, wherein the organic layer affects the electrical property within the silicon-containing material.

15. The process of claim 14, wherein the electrical property is selected from a group consisting of an surface recombination velocity, carrier lifetime, electronic efficiency, voltage, contact resistance, and resistance of a doped region.

16. The process of claim 13, wherein the organic layer comprises a monolayer.

17. The process of claim 13, wherein the organic layer comprises a polymer.

18. The process of claim 13, further comprising doping a portion of the silicon-containing material at the surface, wherein:

    the portion has a dopant concentration of at least approximately $1x10^{19}$ atoms per cubic centimeter immediately adjacent to the surface;

    the silicon-containing material is at least part of a photovoltaic cell; and

    doping is performed before forming the organic layer.

19. The process of claim 13, further comprising forming a gate electrode over the organic layer, wherein:

    the silicon-containing material is at least part of a channel region of a field-effect transistor;

    the organic layer is at least part of a gate dielectric for the field-effect transistor; and

    the gate electrode is a control electrode for the field-effect transistor.

20. The process of claim 13, further comprising:

    forming a high-k material; and

    forming a gate electrode, wherein:

        the silicon-containing material is at least part of a channel region of a field-effect transistor;

        the organic layer lies between the silicon-containing material and the high-k material; and

        the high-k material is at least part of a gate dielectric for the field-effect transistor and lies between the silicon-containing material and the gate electrode.

21. The process of claim 13, wherein forming the organic layer comprises:
    activating the surface of the silicon-containing material to form an activated surface;
    reacting the activated surface with a chemical, wherein during the reaction, a hydrocarbon group becomes chemically bonded to the silicon-containing material.

22. The process of claim 21, wherein activating comprises halogenating the surface of the silicon-containing material to form the activated surface.

23. The process of claim 22, wherein the hydrocarbon group has no more than nine carbon atoms.

24. The process of claim 23, wherein the hydrocarbon group is an alkyl group.

25. The process of claim 21, wherein the hydrocarbon group is an allyl group.

26. The process of claim 21, further comprising forming a polymer layer from the allyl group.

27. The process of claim 21, wherein the hydrocarbon group is an alkoxide group.

28. The process of claim 13, wherein the silicon-containing material is substantially monocrystalline.

29. The process of claim 13, wherein the silicon-containing material is polycrystalline.

30. The process of claim 13, wherein the silicon-containing material is substantially amorphous.

31. A process for forming an electrical device comprising:

forming a patterned insulating layer over at least of the electrical device, wherein:

the patterned insulating layer defines an opening;

a silicon-containing region has an exposed portion at the opening; and

the silicon-containing region is at least part of an electrical component within the electrical device;

forming an organic layer chemically bonded to the surface of the silicon-containing region;

removing the organic layer; and

forming a metal-containing layer after removing the organic layer, wherein at least a portion of the metal-containing layer contacts the exposed portion of the silicon-containing region, and wherein the metal-containing layer is part of an electrical connection to the silicon-containing region.

32. The process of claim 31, further comprising allowing at least approximately four hours to elapse between forming the organic layer and removing the organic layer.

33. The process of claim 31, further comprising annealing the non-insulating layer to form a metal silicide from the metal-containing layer and the silicon-containing region.

34. The process of claim 31, wherein no etching act is performed between forming and removing the organic layer.

35. A process for forming an electrical device comprising:

forming a patterned insulating layer over at least of the electrical device, wherein:

the patterned insulating layer defines an opening;

a silicon-containing region has an exposed portion at the opening; and

the silicon-containing region is at least part of an electrical component within the electrical device;

forming an organic layer chemically bonded to the surface of the crystalline material;

removing the organic layer; and

forming a dopant-source layer that contacts the exposed portion of the silicon-containing region.

36. The process of claim 35, further comprising allowing at least approximately four hours to elapse between forming the organic layer and removing the organic layer.

37. The process of claim 35, wherein the dopant-source layer comprises at least approximately 90 percent of at least one Group IVA element.

38. The process of claim 35, further comprising annealing the dopant-source layer to diffuse at least a portion of the dopant atoms into the silicon-containing region.

39. The process of claim 35, wherein no etching act is performed between forming and removing the organic layer.